Please amend the claims as indicated below:

1. (Currently Amended) A [hardware emulator] system for verifying a plurality of systems on a plurality of chips, said system [emulator] comprising:

a hardware emulator for verifying the plurality of systems on the plurality of chips, said hardware emulator further comprising:

a first circuitry for verifying a first system on a chip, said first circuitry further comprising at least one output for providing testing results from the first system on the chip; and

a second circuitry for verifying a second system on another chip while verifying the first system on chip.

2. (Currently Amended) The [hardware emulator] system of claim 1, wherein the hardware emulator further [comprising] comprises:

a first interface for providing inputs to the first circuitry and receiving outputs from the first circuitry; and

a second interface for providing inputs to the second circuitry and receiving outputs from the second circuitry.

3. (Currently Amended) The [hardware emulator] system of claim 1, wherein the first circuitry is configured to realize the first system on a chip and the second circuitry is configured to realize the second system on another chip.

4. (Currently Amended) A [hardware emulator] system for verifying a plurality of systems on a plurality of chips, said [emulator] system comprising:

a hardware emulator comprising:

a first circuitry configured to realize a first system on a chip, said first circuitry further comprising at least one output for providing testing results

from the first system on the chip; and

a second circuitry configured to realize a second system on another chip while verifying the first system on chip, the second circuitry connected to the first circuitry.

5. (Original) The [hardware emulator] system of claim 4, wherein the hardware emulator further [comprising] comprises:

a first interface operably connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry; and

a second interface operably connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry.

6-11. (Cancelled).